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A Hybrid Topological Flip Flop Design for High Speed and Low Power Applications

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ABSTRACT: Flip-flops are essential parts of digital circuits used to store state data. It is crucial to decrease their power consumption, latency, and area in order to fulfil performance requirements. This study describes a hybrid flip-flop device with eighteen transistors that combines static CMOS logic with pass transistors. It resolves the issue of clock overloading that plagues traditional designs. The hybrid technique makes it possible to achieve the three main goals for flip-flops: high speed, low power consumption, and small size. The proposed circuit is implemented using Tanner Tools and compared with the Transmission gate flip-flop. The hybrid logic architecture that has been suggested has demonstrated the greatest power improvement that is, 19.9 μ W when compared to TGFF.

KEYWORDS - CMOS, low power, flip-flop, complementary pass transistor.

I. INTRODUCTION

A flip-flop is a basic storage element that is frequently utilised in digital system designs. In low power electronics applications like smartphones, tablets, mobile phones, and other handheld devices, the flip-flop is widely employed. For a while every gadget should have a long battery life and little power consumption. Memory unit latency should also be kept to a minimum for quick processing performance. The clock system in digital hardware circuits accounts for 20% to 40% of the integrated circuit's (IC) overall power consumption. Through the use of several low power approaches, flip-flop designs are continuously improved. The most popular industry standard flip-flop is the Transmission Gate flip-flop (TGFF). Clock overloading is the main issue with these designs. These flip-flop logic structures are made up of the CLK and CLK bar clock signals, respectively. These signals raise the number of transistors in addition to increasing the clock signal's workload. Because more circuitry is needed to generate the CLK and CLK bar signals, there are changes to the overall design structure. This resulted in a notable rise in dynamic power losses, even during periods of low data switching activity. These days, the two main issues for VLSIs are production costs and chip area.

This brief describes the design of a flip-flop using hybrid logic. In comparison to the current M-S flip-flops, the suggested flip-flop structure tackles the notable improvement in (1) Clock to Q delay. (2) This work also avoids clock overloading, which contributes to a lower power usage. (3) A decrease in the number of PMOS transistors, which lowers the circuit's total power, area, and latency. Reducing the total intricacy. All of the results were obtained using Tanner tools at room temperature and 250nm UMC CMOS technology with a maximum supply voltage of 0.5 V.

II. EXISTING METHOD

Transmission gates and inverters make up the TGFF. A master-slave setup is used. Two transmission gates operated by an inverted clock and a clock that is attached to the input data line make up the master latch. These enable the input data to be sampled by the master on the clock's rising edge. When the clock is low, the two inverters that the master drives maintain the state. Transmission gates are also used by the slave latch to collect the master output when the clock's falling edge occurs. The ultimate output inverter is powered by the slave. The fact that 12 transistors are clocked results in significant clock loading, and contention current occurs when both transmission gates are partially on during transitions.

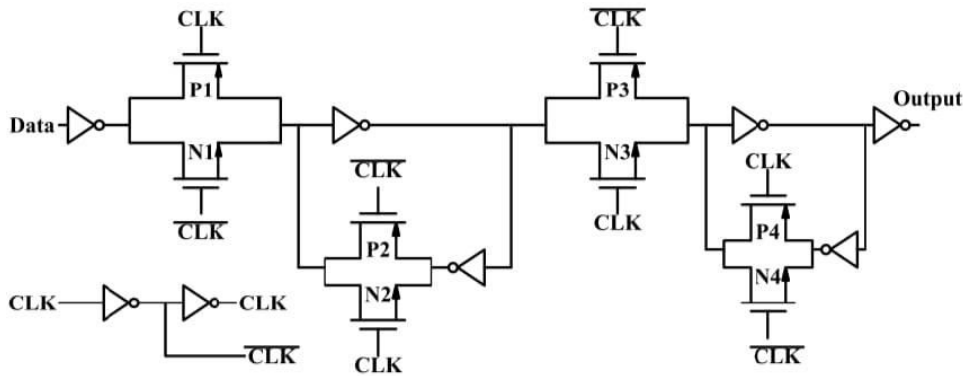
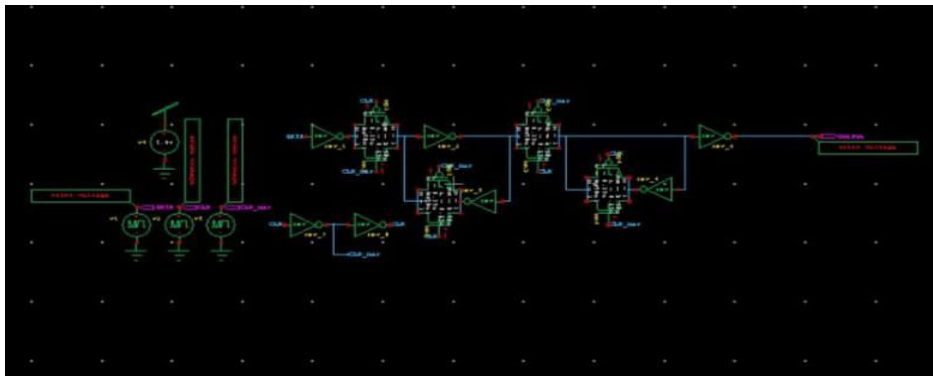


FIGURE 1:BLOCK DIAGRAM OF TGFF



DESIGN OF TRANSMISSION GATE FLIP FLOP

III. PROPOSED FLIP-FLOP DESIGN

In order to minimise latency, minimise circuit complexity, and optimise power consumption, we have logically and topologically decreased the number of transistors, particularly PMOS transistors. We have reduced the continuous 2 PMOS transistors in the same path from VDD to GND because of the limited mobility of the PMOS transistors. As a result, the proposed flip-flop has less delay. Furthermore, because the suggested design has a simpler circuit than the LRFF, it takes up less space. Our suggested design, known as a hybrid flip-flop (HFF), is seen in Figure. Since it also includes a balancing clock and logic reduction, LRFF and ACFE are both included in the suggested hybrid construction, which satisfies the specifications with just 18 transistors. Four pass transistors (P2, P3, N6, and N7), two NMOS to store data in master transistors, and six inverters make up the hybrid topological structure. Of the four pass transistors, one pair acts as an auxiliary transistor (AT) to provide either a strong 1 or a weak 0. The other pass transistor pair functions as a current booster (CB).

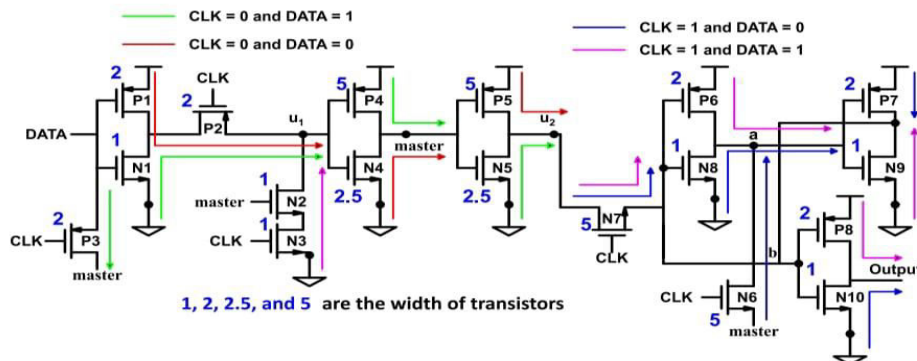
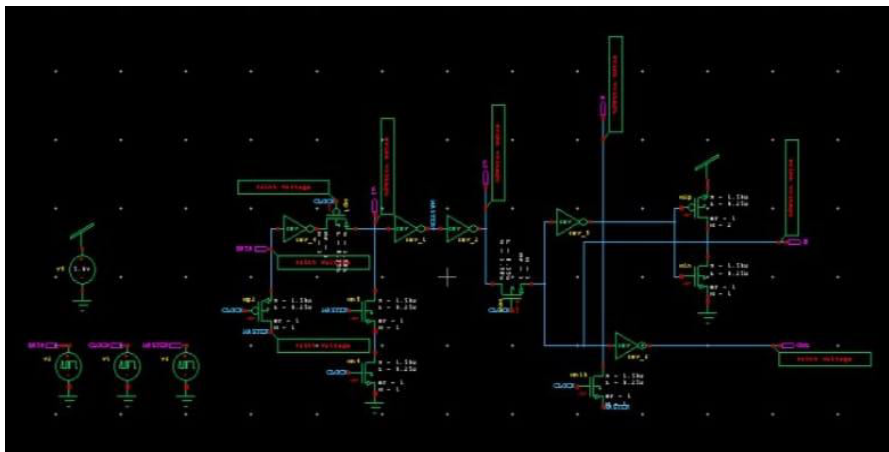


FIGURE 2:BLOCK DIAGRAM OF PROPOSED METHOD



DESIGN OF PROPOSED METHOD

A. Cases of Data Latching

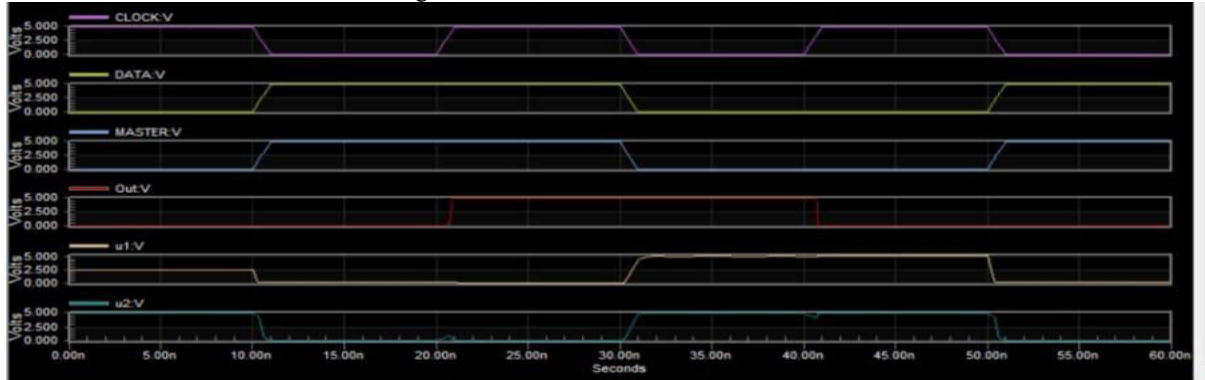
- 1) Situation (Clock = 0 and Data = 0): Node "u1" equals 1 when CLK = 0 and DATA = 0, so P1, P2, and N4 transistors will be in the ON state. However, since transistors N6 and N7 are off, neither the "master" node nor node u2 will be able to send any data to the slave latch. Slave will therefore retain its prior value at the output node. Transistor P3 acts as an AT in this situation since it passes weak 0 at the "master" node. Since the transistor P2 passes a strong 1 that satisfies the logic 0 at the master node, it acts as a current booster.
- 2) Case (Data = 0 and Clock = 1): Transistors N6 and N7 will be in the ON state when CLK = 1 and DATA = 0. Slave nodes "a" and "b" receive data from the "master" and "u2" nodes via N6 and N7, respectively. This uses the slave to supply the data at the output. N6 is a CB when the master node output is 0 because it passes strong "0" at node "a." N7 is an AT at the same time since it passes weak "1" at node "b"
- 3) Case (Data = 1 and Clock = 0): transistors N1, P2, and P4 will be in the ON state when CLK = 0 and DATA = 1. This causes node u1 and u2 to be pulled to logic "0," but the master node keeps the data at logic "1." At the output node, the slave will retain the value it had before. Transistor P2 acts as an AT under these circumstances, passing weak 0 at node u1. Transistor P3, on the other hand, acts like a CB since it passes strong 1 at the master node.
- 4) Situation (Clock = 1) and Data = 1): Similar to the example above where CLK = 1, logic at the master node will be passed to the slave when CLK = 1 and DATA = 1. N7 acts as a CB when the master node output is at logic "1," passing strong "0" at node "b" N6 acts like an AT at the same time since it passes weak "1" at node "a."

IV. EXPERIMENTAL RESULTS

A. Output Waveform

Clock, Data and Master are the inputs, clock and data are the primary inputs and master behave as input to transfer the data to slave. Here when CLK=0,DATA=0 and MASTER =1,no data will be transferred.when CLK =1,DATA =1

and MASTER =0,data will not transferred to slave node but data will be hold. when CLK =1,DATA =1 and MASTER =1, data will transfered to slave node through master node.



B.Power, Area and Delay

PARAMETERS	TGFF	HFF
Power	20.90(μW)	1.00(μW)
Transistors	22	18
Delay	0.88sec	0.52sec

HFF turns out to be the most practical and efficient option when TGFF and HFF are compared across power, area, and delay factors, according to the data presented. With a power consumption of only 1.00μW as opposed to TGFF's 20.90μW, it offers superior energy efficiency. Furthermore, HFF takes up less space (18 units) than TGFF (22 units), indicating a more compact design that is beneficial for lowering production costs and enhancing device integration. In addition, HFF performs better than TGFF with a delay time, which makes it speedier and more appropriate for situations where speed is crucial. Overall, HFF is a better choice for a variety of applications due to its smaller size, quicker processing, and reduced power consumption.

C. Variation of Power With Supply Voltage

Figure shows the power consumption level at various supply voltages between 0.5 V and 1 V. Among state-of-the-art work, the HFF has the lowest power consumption and functions correctly at this voltage range. This is because there are fewer transistors on the critical path of the suggested flip-flop. This is accomplished by eliminating PMOS from the circuit without compromising its operation.

V.CONCLUSION

The design of a new flip-flop made with Eighteen transistors. The following criteria have been taken into consideration for the proposed work: C to Q latency, reduction in PMOS transistor count, reduced circuit complexity, and absence of clock overloading. In comparison to TGFF, the HFF circuit performed better in terms of power consumption by 1.02μW respectively. It performs exceptionally well across the supply voltages and is free from clock overloading. Every parameter that was used for this task has been effectively addressed. The proposed method and power consumption is decreased by 19.90μW.

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